A Design Methodology of MMIC Power Amplifiers Using AI-driven Design Techniques

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***Abstract*—The design of a monolithic microwave integrated circuit (MMIC) power amplifier (PA) is challenging since it involves multiple stages with tens of parameters and several types of simulations. Therefore, artificial intelligence (AI) techniques are attracting much attention for PA design. This paper presents an AI-driven design methodology for MMIC PAs design incorporating the surrogate model-assisted global optimization algorithm, data-flow interface, and simulators. The methodology is verified on a practical 3-stage PA design case operating in 27-31 GHz, containing 30 variables. The case is synthesized successfully without the need for any initial solution and shows good in-band performance consistency, which paves the way for future AI-driven PA design applications.**

***Index Terms*—artificial intelligence, power amplifier, global optimization, millimeter-wave**

I. Introduction

The widespread demand for high data-rate communication systems has led to the rapid development of millimeter-wave (mm-wave) technology aiming for 5G or satellite communications and remote sensing. One of the critical components of mm-wave front-ends is power amplifier (PA), which elevates the power of small RF signals to an antenna for radiation. The integration of PA composed of both driver and final stages into monolithic microwave integrated circuit (MMIC) technology has the potential to provide a compact and cost-effective solution for mm-wave PA design. Thus, much attention has been focused on mm-wave MMICs design in recent decades.

However, the design of MMIC PAs is a complicated process involving multiple steps. Engineers should first select the proper technology of transistor (e.g., by LDMOS, GaAs, or GaN technology) with enough margin for output power and efficiency. Then determine the gate length and finger number for different stages (e.g. driver and final stage). Due to the intrinsic non-linear property, designers should carefully choose the input and output impedance for different stages in distinct power levels by conducting load-pull/source-pull simulations. With selected transistors, a full EM simulation of input/inter/output matching networks is implemented to characterize the PA performance, such as operating bandwidths, output power, efficiency, gain, and linearity. It usually takes many iterations from the transistor selections to the EM simulation to update the design and make a trade-off between various PA requirements. It is time-consuming and might be highly experience-relied. In addition, achieving an optimal PA performance is quite challenging since there are strong interactions between different design parameters. Hence, AI-driven design techniques are considered to be used in the PA design domain.

Reported AI-driven PA design can be categorized into two types: topology design and parameter design. Topology design uses AI techniques to determine the structure of matching circuits, while parameter design optimizes the value of components. In [1], the authors presented an automated DNN-based 1-stage PA design technique consisting of both two design types, called topology determination and value estimation. A DNN classifier is utilized to predict the number of lump elements used in the input and output circuit, while a regression model is employed to optimize parameter values with the help of Thompson sampling. However, the design process is load-pull data-based considering no large-signal simulation, and the topology is predefined by lumped elements, which inevitably restricts its application. Besides [1] which combines topology and parameter design, more methods mainly focus on parameter design, on which this paper focuses.

In recent years, several optimization-based methods are proposed for the parameter design of PA. [2] and [3] utilized a simulated annealing particle swarm optimization (SA-PSO) method for the design of high-efficiency PA and broadband Doherty PA, respectively. However, it is a pure-heuristic and model-free method, thus taking rapid growth of computational cost for complicated cases, especially considering electromagnetic (EM) simulations. To address the long computing time, [4] considers a bayesian optimization (BO) framework for broadband high-efficiency PAs and later also extends to a multiobjective scenario [5]. BO framework uses the gaussian process model for predicting the best new solution in each iteration, helping to reduce the necessary number of EM simulations. Nevertheless, due to the lack of search operators, the initial design is always needed and its quality largely affects the performance of the final solution.

Additionally, the above-mentioned methods are proposed for only one stage design, thus are not appropriate for MMICs (chip-level synthesis). In [6], an algorithm for general mm-wave ICs' design (GASPAD) is proposed and provides a feasible solution. A gaussian process (GP) surrogate model cooperated with differential evolution is embedded into the synthesis method enabling global search without the need for the initial design. Although GASPAD is only validated on small-scale CMOS ICs with design variables of around 15,

it shows promise in chip-level synthesis.

To the best of our knowledge, most existing AI-driven design research in the literature focus on algorithmic innovation, and a systematic description of the AI-driven design process is somewhat insufficient. In this paper, we present an AI-driven MMIC PAs design methodology, involving the problem formulation, the data flow between the core optimizer and the simulator as well as its implementation. The case study is a design of 3-stage PA including two kinds of simulation, i.e., EM simulation (for microstrip lines and metal-insulator-metal (MIM) capacitors and thin-film resistor (TFR)) and harmonic balance simulation (i.e. for PA transistors and layout).

The remainder of this paper is organized as follows. In Section II, the design problem is formulated, the design data flow diagram is illustrated, and the optimization algorithm is explained in detail. Section III shows the case study designed by the proposed method. Conclusions are finally provided in Section IV.

II. AI-driven MMIC PAs Design Methodology

A. Formulation of Design Problem

MMIC PAs design can be treated as a constrained black-box optimization problem formulated as follows:

$$\begin{aligned} \min_{\boldsymbol{x}} \quad & f_0(\boldsymbol{x},\omega) \\ \text{subject to} \quad & f_i(\boldsymbol{x},\omega) \le 0 \quad \text{for } i=1,...,m \\ & \boldsymbol{x} \in [LB, UB] \\ & \omega \in [\omega_1, \omega_2] \end{aligned} \tag{1}$$

where x is a d-dimensional vector of design variables, LB and UB are lower and upper bound, respectively, and ω indicates the operation band with desired performances. $f_0(\boldsymbol{x},\omega)$ is the objective metric aiming to minimize under multiple constraints' metrics $f_i(\boldsymbol{x},\omega)$.

$f_0(\boldsymbol{x},\omega)$ and $f_i(\boldsymbol{x},\omega)$ are always obtained by simulation. For instance, $f_i(\boldsymbol{x},\omega)$ can be the minimum input return loss (known as S_{11}), the minimum small-signal gain (known as S_{21}), the minimum output power or efficiency at 3-dB gain compression point, or the maximum amplitude modulation to phase modulation (AMPM) degree in a band. In practice, performance metrics are always on different scales. Thus, each metric should be normalized as follows:

$$f_i(\boldsymbol{x}) = \frac{y_i - y_i^{spec}}{y_i^{ref} - y_i^{spec}} \tag{2}$$

where y_i is the real value obtained from simulations, y_i^{spec} and y_i^{ref} are specification and reference value, respectively. Note that Eqn. (2) concurrently transforms all the metrics into the minimization direction, which greatly facilitates the subsequent optimization process. To deal with the objective subjected to various constraints, in this work, a penalty function is defined for optimization

$$F(\boldsymbol{x}) = f_0(\boldsymbol{x}) + \sum_{i=1}^{m} \max(0, w_i \cdot f_i(\boldsymbol{x})) \tag{3}$$

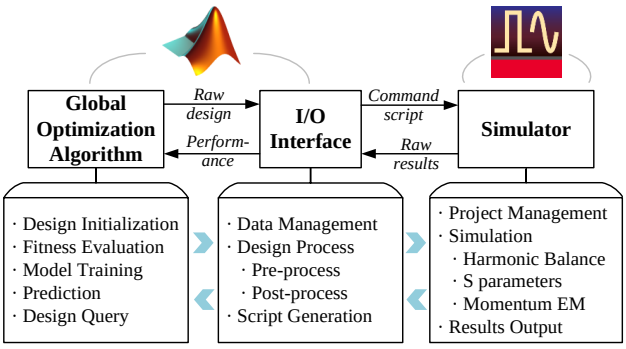

Fig. 1. Data flow, functions, and diagram.

where w_i is the weighting factor. $\max(\cdot)$ clipping is used to prevent violation of any constraints. The penalty function value describes the integrated quality or performance of designs. The AI-driven design process in the following aims to solve the above-formulated problem.

B. AI-driven Design Data Flow

To achieve AI-driven design procedures, the algorithm should cooperate with electronic design simulation software (simulator). Therefore, an input and output (I/O) interface is needed. As depicted in Fig. 1, there are three building blocks: the algorithm container, I/O interface, and simulator. The algorithm controls the whole design optimization process, including initializing the design space, training the model, predicting the design performance, and recommending the next candidate with the best potential. The interface takes the raw design vector and quantizes it to the appropriate grid, the so-called preprocess. Then the command scripts are generated to revise the component values of the design parameters and launch a series of simulations. The simulator manages the project and executes specific simulation tasks, such as harmonic balance, S-parameters, and momentum-based EM simulation. The simulator then exports raw results regarding performance versus frequency to the interface, which post-processes them into a recognizable format by the optimizer for evaluation.

In this work, Advanced Design System (ADS) is employed as the simulator. ADS is a popular tool for MMIC design and is supported by most of the foundry companies with useful Process Design Kits (PDKs). For the optimization algorithm and I/O interface, MATLAB programs are implemented. AEL scripts are generated to control ADS simulations.

C. SAEA-based Optimization Algorithm

As mentioned above, GASPAD is introduced and serves as the optimizer in this work. The core of GASPAD is a surrogate model-assisted evolutionary algorithm (SAEA), which overcomes at least the following two difficulties in MMIC PA design applications: (1) Reduce the number of computationally expensive simulations. (2) Introduce global exploration ability during optimization. The algorithm is explained in this subsection.

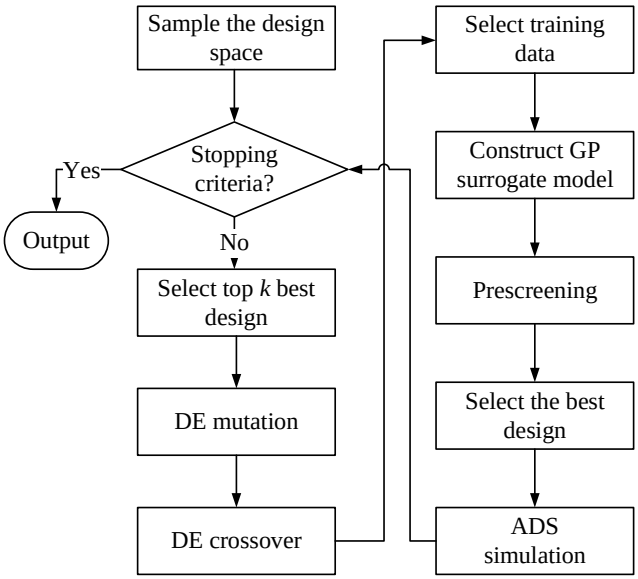

Fig. 2. Optimization algorithm flow.

The framework of the optimization algorithm is shown in Fig. 2. Specifically, Latin hypercube sampling (LHS) is first employed to initialize the design space within given intervals. Meanwhile, all samples are simulated in ADS and the performance results are stored in the database. In each iteration, designs are sorted by their penalty function value calculated by Eqn. (3), while only the top k of them are selected to form the population. Next, differential evolutionary (DE) operations including mutation and crossover are performed to generate a child population. To predict the quality of all child designs, $m+1$ GP models for different design metrics (i.e., $f_i(\boldsymbol{x}), i = 0, \ldots, m$) are constructed based on selected training data. Moreover, by applying the prescreening method to the predictions, only the child design with minimal prescreening value is selected. The design is then simulated, and updated in the database for the next iteration. This loop will terminate once the specification or other stopping criteria are met.

There are three details to be clarified in the proposed algorithm: the manner to perform mutation and crossover operations, the way to select training data, and the method to perform prescreening.

The manner of mutation and crossover introduces population diversity which directly relates to the algorithm's capability of exploration. To balance them, DE/current-to-best/1, a middle strategy of mutation is utilized

$$\boldsymbol{v}_i = \boldsymbol{x}_i + F \cdot (\boldsymbol{x}_{best} - \boldsymbol{x}_i) + F \cdot (\boldsymbol{x}_{r_1} - \boldsymbol{x}_{r_2}) \tag{4}$$

where $\boldsymbol{x}_{best}$ is the best design, $\boldsymbol{x}_{r_1}$ and $\boldsymbol{x}_{r_2}$ are two randomly selected designs in the current population, and F are scaling factor. $F \in (0, 2]$ is set to be a constant in this work. The crossover operator parameterized by CR is set the same as in [6].

Inspired by the idea of surrogate model-aware evolutionary search [6], a distance-based training data selection method is utilized to ensure optimization ability in a promising subregion. In each iteration, the nearest $5d$ designs (Euclidean distance) in the database to the centroid of the child population (mean value of designs in child population) are selected as training data. This method restricts the model to a smaller dynamic region compared to others and improves the ability of exploitation. Note that only a single surrogate model considering one metric is constructed and applied to all child designs, which reduces the modeling time for the increasing number of design variables.

As for prescreening, the lower confidence bound method (LCB) is used. Mathematically,

$$f_{lcb}(\boldsymbol{x}) = \hat{f}^(\boldsymbol{x}) - 2\hat{s}(\boldsymbol{x}) \tag{5}$$

where $\hat{s}^2$ is the predictive uncertainty value obtained by GP model. LCB method provides a flexible control on exploration and exploitation and promotes global search during optimization.

Note that no initial design is needed at the beginning. The requirement for experience from engineers is thus highly reduced.

III. Case Study

The design of a practical MMIC PA based on OMMIC GaN-on-Si technology is presented as a case study in this section. The design case consists of three stages: two driver stages and one balanced final stage. The MMIC PA is supposed to operate over 27-31 GHz covering 5G FR2 bands n257 and n261. All specifications shown in Table I are designated to meet recent market development requirements, such as power-added efficiency (PAE) and power output (Pout).

TABLE I
Design specifications for power amplifier case

Type	Item Description	Frequency Range	Specification
Objective	Bandwidth	-	$\geq$ 4GHz
Constraint 1	Input Matching	27-31 GHz	< -11dB
Constraint 2	Output Matching	27-31 GHz	< -11dB
Constraint 3	Total Gain	27-31 GHz	$>$ 16dB
Constraint 4	Gain Imbalance	27-31 GHz	$<$ 1dB
Constraint 5	PAE	27-31 GHz	$> 22\%$
Constraint 6	Output Power	27-31 GHz	$>$ 32dBm

For the convenience of verifying our algorithm, all stages are integrated into one schematic, as shown in Fig. 3. The transistors are simulated by the Harmonic Balance simulator based on compact models provided by the foundry. The harmonic order is set to 5 to ensure enough nonlinear characterization capability. The MIM capacitors, TFR components, and microstrip lines are simulated by the Momentum EM simulator based on the substrate model provided by the foundry as well. The simulation frequency range is set from 0-150 GHz to cover the quintic fundamental frequency range. All constraints in Table I are metrics regarding frequency, exported from ADS. A complete simulation takes about 700 seconds.

There are 30 design variables that can be categorized into four types: (a) capacitor value, (b) line width/length, (c) finger

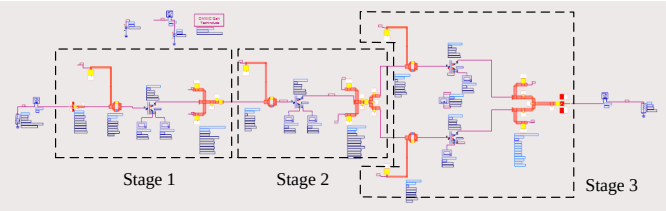

Fig. 3. Schematic of the MMIC PA.

number, and (d) gate length, as presented in Table II. All parameters are quantized into their grids by considering the feasibility of simulation and processing. The search bounds UB and LB are roughly set to a wide range, i.e., no initial design is needed.

TABLE II
TYPE, NAME, DESIGN BOUNDS, AND THE OPTIMIZED SOLUTION

Type	b	a	b	a	b	a	b	a
Name	L1	C1	L2	C2	L3	C3	L4	C4
UB	30	600	500	500	50	2000	50	500
LB	3	50	50	80	3	200	3	50
Opt.	8.5	273.7	195.5	137.1	29	2000	81	267
Type	b	b	b	a	b	a	b	a
Name	L5	L6	L7	C5	L8	C6	L9	C7
UB	300	500	300	500	100	500	200	500
LB	3	5	10	30	3	20	3	50
Opt.	46.5	68	10	241.4	78.5	200.7	64	135.8
Type	b	b	a	b	a	b	a	b
Name	L10	L11	C8	L12	C9	L13	C10	L14
UB	100	300	500	800	500	500	300	300
LB	3	10	50	50	30	50	50	50
Opt.	86	32	97.8	172	145.2	260.5	70.9	218
Type	d	c	d	c	d	c		
Name	W1	N1	W2	N2	W3	N3		
UB	100	8	100	8	100	8		
LB	40	4	40	4	40	4		
Opt.	100	6	75	6	45	6		

For parameter settings of the algorithm, the k is set to $5d$, i.e., 150 in this case, while F and CR in DE operation is set to 0.8 and 0.6, respectively. All constraints are equally considered, which means w is a all one's vector. Meanwhile, the simulation budget is set to 2000. The optimized design of one run is exhibited in Table II **Opt.** row, while its performance is shown in Fig. 5. It takes 1989 iterations to achieve this result. Due to time limitations, the algorithm was only run once. As a comparison, the design obtained by ADS built-in optimizers is far from the specifications.

As for the performance of this design, it is found that all constraints are satisfied and the minimum objective requirement, i.e., 4 GHz operation bandwidth, is achieved. The layout of this MMIC is shown in Fig. 4.

IV. CONCLUSION

In this paper, an AI-driven design methodology for MMIC PAs is systematically presented and verified by a practical case. Remarkably, the case contains 30 variables and no initial design is needed. Successful results are obtained after

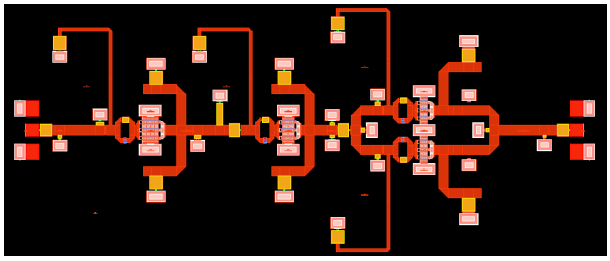

Fig. 4. Layout of the optimized MMIC PA.

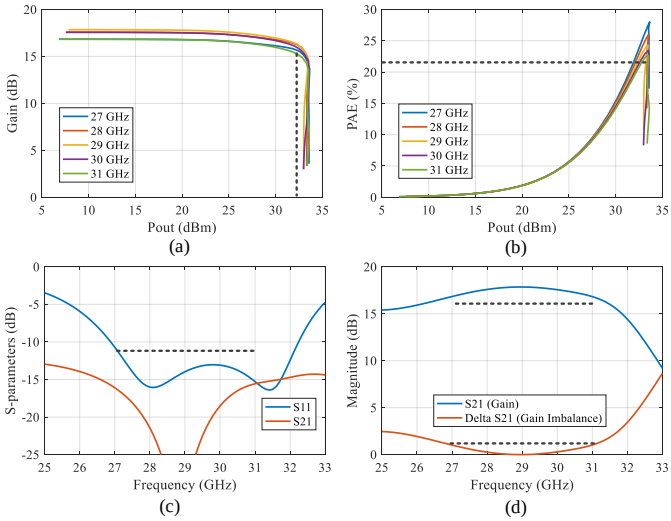

Fig. 5. Performance of the optimized design.

optimization, in which all constraints are satisfied and the bandwidth is extended to be more than the required 4 GHz. Since there is no initial design needed, the experience needed from engineers is highly reduced. This methodology shows high potential in terms of effectiveness and design quality for MMIC PAs' design.

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