A novel high-performance V-band GaN MMIC HPA for the QV-LIFT project

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Joël Moron, Rémy Leblanc, Peter Frijlink, François Lecourt
OMMIC sas, 2 chemin du Moulin - 94453 Limeil Cedex, France
Tel. +33.145105442, Fax +33.145106953, J.Moron@ommic.com
Manuel Sigler
ERZIA Technologies, Josefina de la Maza 4, 39012, Santander, Spain, Tel: +34 942 29 13 42, manuel.sigler@erzia.com
George Goussetis
School of Engineering and Physical Sciences, Heriot-Watt University, Earl Mountbatten Building 2.26, Edinburgh, EH14 4AS, UK, tel: +44(0)131-451-3055, g.goussetis@hw.ac.uk
Giandomenico Amendola
CNIT-Università della Calabria, +39 0984494611, g.amendola@dimes.unical.it
Giuseppe Codispoti, Giuseppe Valente, Giorgia Parca
Agenzia Spaziale Italiana, Via del Politecnico snc, 00133, Rome, Italy, +39 06 8567.1
giuseppe.codispoti@asi.it, giuseppe.valente@asi.it, giorgia.parca@asi.it

Abstract

This paper reports the development of a V-band Gallium Nitride (GaN) Monolithic Microwave Integrated Circuits (MMIC) high power amplifier in the framework of the Horizon 2020 project QV-LIFT. Design manufacturing and on-wafer pulsed measurements of the first run were performed by OMMIC and demonstrate peak output power of about 5W. ERZIA Technologies has designed the connectorized module for Continuous Wave (CW) characterization of the circuit and has performed the measurements of the module, demonstrating RF power in excess of 3 W at the satellite V-band. Overall experimental measurements are in line with the theoretical predictions and they represent state of the art.

1. Introduction

Future satellite communication systems are required to satisfy the increasing demand for satellite-delivered global broadband services. Market trend has been shifting from TV broadcast dominated services to multi-service communications and in particular to broadband connectivity and Internet access services, resulting in a new set of system requirements for satellite systems.

The strategy adopted by next generation high throughput architectures foresees the exploitation of EHF as a key enabler for the “Terabit connectivity” and in particular the Q/V band has been proving capabilities and promising perspectives for the feeder link implementation.

The QV-LIFT project [1], funded by European Commission under the Horizon 2020 program (Grant Agreement No. 730104 H2020-COMPET-2016), aims at developing the foundation of the Ground Segment Technology for the future Q/V band Terabit SatCom systems. Q/V band frequencies (40 GHz for downlink and 50 GHz for uplink) offer larger bandwidth availability for the feeder links and for specific segments requiring high data rates. The project aims at providing key

Ground Segment technologies and strategies able to support the future Q/V feeder links, thus contributing to fill the technological gap on components and terminals with good performance at Q/V band [2].

Within QV-LIFT, the final goal is to implement a test environment based on the use of the operational payload "Aldo Paraboni", on board of Alphasat Satellite, and its Ground Stations, thus allowing to test a full satellite link between gateway and user terminal, either at hardware and network level [3].

Due to high performance required and high frequency of operation, up to date technologies are needed to realize main RF components.

In particular, the objective of this paper is to present one of the key objectives of the project, which is the development of the QV-LIFT High Power Amplifier (HPA), based on the design, the fabrication and the evaluation of a Gallium Nitride based power amplifier MMIC that can be used at ground terminals transmitting at V-band.

Two runs of MMIC fabrication are scheduled as part of the development process. The best chipsets will be then integrated in a 4-way combiner for the final Solid State HPA, targeting 10 W combined RF output power.

This paper presents results of the first run, which has been completed and tested. On wafer measurements indicate performance with gain 17dB and output power in the range 36 to 37 dBm at 47/48GHz, which is worldwide state of the art for an MMIC. An HPA manufactured by mounting a single MMIC on a board presents a behaviour as expected in terms of output power (measured at about 35 dBm at 4 dB compression at 48.6 GHz), gain (16 dB at 48 GHz), and power consumption (26.5 W at saturation). Presently, the second run of MMIC design is being undertaken to fine tune this performance.

2. MMIC HPA for the QV-Lift project: design and development

2.1 MMIC process

For the Power Amplifier MMIC required for the QV-LIFT uplink, it has been decided to use the commercial 100 nm GaN on Silicon process open for foundry runs by OMMIC. The process has been available for several years and is fully industrial. It includes a passivation and protections with several SiN and thick SiO2 dielectric layers, and is thus compatible with plastic packaging with low impact of the molded material.

The main features of the process are:

- 100 nm mushroom gate Normally ON pHemt transistors
- MIM capacitors (400 pF/mm^2 and 50 pF/mm^2) - Resistors (40 Ω/ mm^2 and 400 Ω/ mm^2)
- Air bridges - thick interconnect metal - via holes through the substrate for RF grounding.

The electrical characteristics of this process relevant to millimeter wave power amplifiers, as documented in the OMMIC GaN Design Manual, are shown in Table 1

Table . The proposed design kit includes transistor electro-thermal non-linear model, scaled model for all passive devices, auto-layout, electromagnetic simulation environment and Design

Rule check. Noise and switch models are also available, making possible the integration of multiple functions used in RF front-ends.

Electrical Characteristic	Value
Frequency Cutoff	105 GHz
Maximum Stable Gain at 30 GHz (2x25µm transistor)	13 dB
RF power density	3.3 W/mm
Extrinsic Transconductance	800 mS/mm
Extrinsic Drain Source resistance Vds=0V	0.6 Ω.mm
Breakdown voltage at 300µA/mm	50 V
Maximum Drain Current at Vds=3V	1.3 A/mm
Recommended Quiescent VDD	12 V

Table 1 D01GH GaN/Si process electrical characteristics

2.2 MMIC Design

The design of this amplifier implied two challenges:

- The 48 GHz frequency range, unusually high for a GaN process, for which we target a minimum small signal gain of 16 dB and a 5 W (37dBm) output power
- The control of the dissipated power, taking into account the Si substrate which has a higher thermal resistance than SiC, together with the reliability requirements of industrial applications.

At microwave frequencies, the transistor environment is constrained: the source is connected to via holes presenting an impedance of approximately 6 Ohms for a 20 pH inductance at 48 GHz, to be compared with the 0.2 Ohms.mm source resistance of the transistor. A series feedback is created, reducing the gain when the total gate periphery is increased. To keep enough gain to allow compression, a unit transistor cell of 6 x 85 µm = 510 µm was chosen by simulation to reach at least 6 dB small signal gain in optimum power match conditions and deep AB class of operation. With 3.3 W/mm of RF output power and 1 dB loss in the combiner, the target of 5 W (37 dBm) can be reached by the combination of 8 transistors in the output stage, including a 2dB additionnal margin for various simulation/reality discrepancies.

Taking into account the losses of the matching networks and of the output power combiner, a 4 stages topology has been chosen to reach the 16 dB small signal gain.

The maximum dissipated power density to keep the hot spot temperature at 200°C for 80°C backside (120 °C increase) is approximately 3.5 W/mm. This temperature ensures an MTTF of 106 hours compatible with industrial applications. The dissipated power is defined in (1).

$$PDISS = PDC + PIN - POUT \quad (1)$$

where PDISS is the dissipated power, PDC is the DC power, PIN is the input power and POUT is the output power of this transistor. This dissipated power is calculated during the design optimization and kept as low as possible through the choice of the load line and class biasing.

Loadpull simulations on the unitary transistor are used to choose the load impedance that will provide the best trade-off in terms of:

- RF power / Power added Efficiency
- Small signal Gain
- Dissipated Power / channel temperature.

All passive networks (output combiner and interstage splitters) are designed to provide this optimimum load to each transistor.

Individual stages have been designed to be stable for each biasing point along the load line up to the Maximum Available Gain cut-off frequency of the transistor (200 GHz). To avoid odd-mode and parametric oscillations, additionnal analysis were done, using the pole and zero analysis package described in [4], and balancing resistors have been added where needed in parallel to each branch of the power amplifier.

The final layout is shown on Figure 1. The circuit size including the dicing street is 3.7 x 2.8 mm^2.

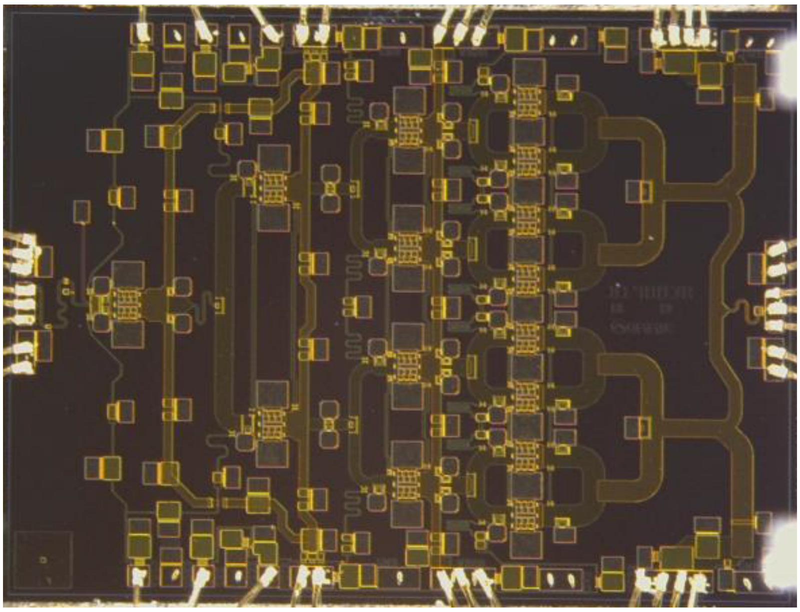

Figure 1: Photograph of the 48 GHz GaN amplifier

3. Measurements

After manufacturing, the MMIC has been measured directly on wafer using Ground-Signal-Ground microwave probes and dedicated DC probe cards. In these on-wafer test conditions the thermal contact of the backside of the chip on the heat sink is poor, so that the test has been performed in pulsed operation, with a 9 µs pulse width and 1% duty cycle to avoid prober chuck heating.

As shown on Figure 2, the measured small signal gain is above 16 dB from 45.5 to 47.2 GHz, the output power at 4 dB compression (Figure 3) is above 37 dBm from 47 to 47.5 GHz.

A test fixture (Figure 4 - left) has been designed by ERZIA Technologies for Continuous Wave (CW) measurements. This module provides:

- The proper heat dissipation from the back-side of the die to ensure channel temperature below +200 °C
- RF interfaces for low losses and 50 Ohms input/output matchings.
- DC biasing and decoupling for good stability at low frequencies

CW measurements (Figure 4 - right) have been performed by ERZIA Technologies and give more than 35 dBm at 48 GHz. From on-wafer, the peak of RF power is shifted by roughly 1 GHz toward higher frequencies (48.5 GHz), which can be explained by a better output load presented to the PA, with respect to simulations conditions. The difference of RF power level, around 35 dBm compared to 36.5 dBm on wafer, is consistent with:

- 1 dB losses of output alumina and connector
- Higher channel temperature

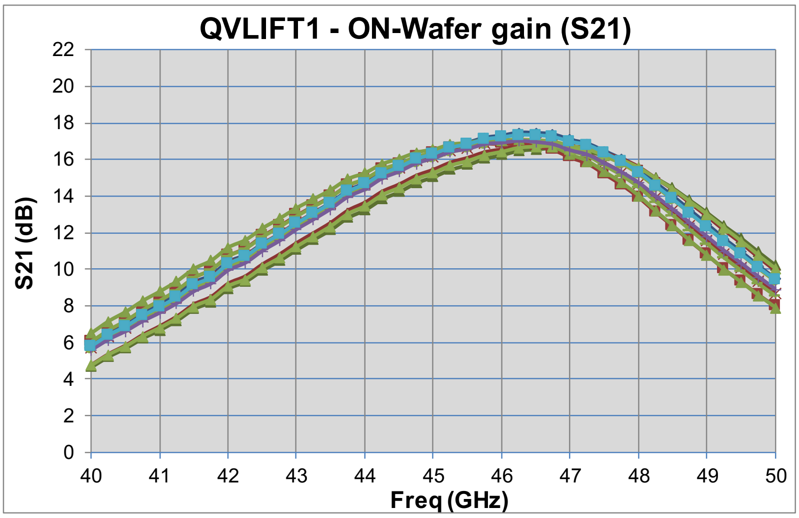

Figure 2: On Wafer S-parameters measurement – S21

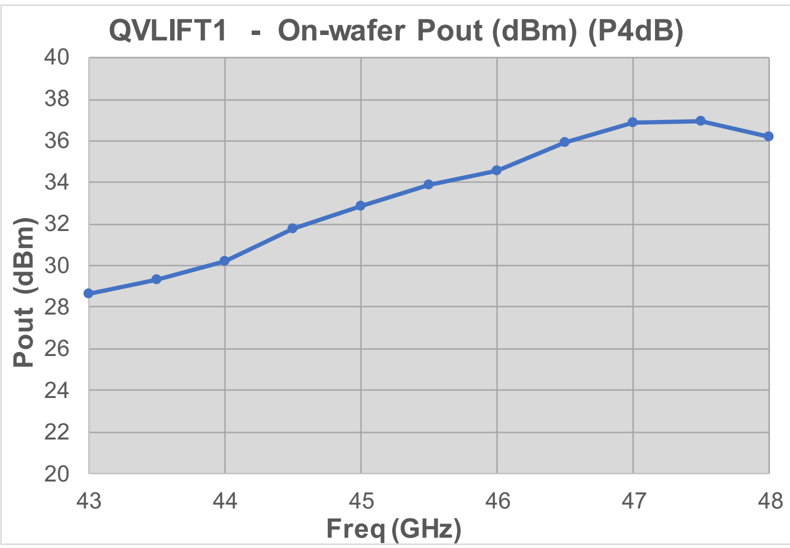

Figure 3: On-Wafer Output Power (dBm) at 4 dB compression

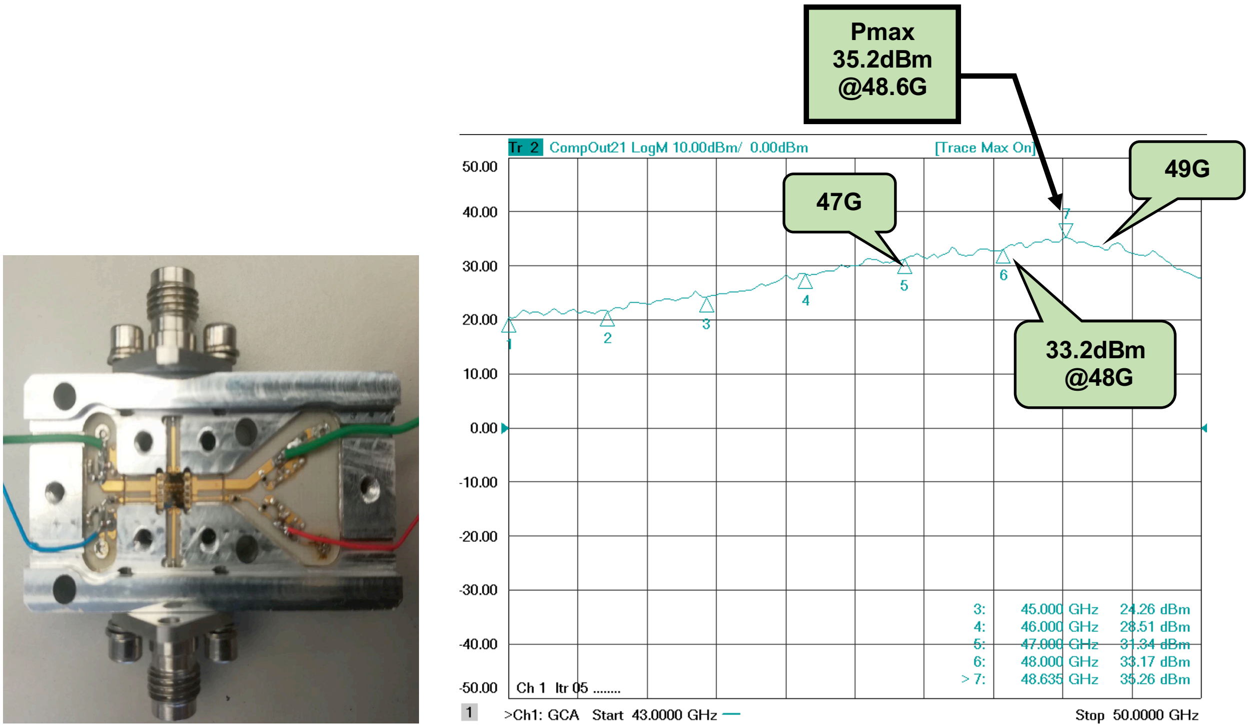

Figure 4: CW Test fixture (left) and Output Power (dBm) at 4 dB compression (right)

4. Conclusion

A MMIC power amplifier based on an industrial GaN on Silicon process by OMMIC has been designed and fabricated. The manufactured MMIC was measured on wafer, as well as mounted on a test fixture. On wafer measurements indicated peak output power of about 5 W, while the mounted amplifier deliver power in excess of 3 W at the satellite V-band. Within anticipated discrepancies due to experimental uncertainties, the measurements match well the simulated results. This MMIC is the first run of the V-band GaN power amplifier development of the QV-LIFT project. This first version of HPA is very close to the specifications targeted in the frame of QVLIFT project and can already be used to conduct the first experimentations of the data link with the satellite. A second run is currently under development targeting to further optimize the performance.

Acknowledgements

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