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Experimental up-scaling of thermal conductivity reductions in silicon by vacancy-engineering: From the nano- to the micro-scale

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Abstract

A method to reduce the thermal conductivity in Si thin-films by at least an order of magnitude is shown, successfully demonstrating the up-scaling of this technique from Si nano-films. High energy self implantation of Si is used to create a supersaturation of lattice vacancy concentrations that remain following post implant rapid thermal annealing producing a disruption in phonon mode thermal transport. This method demonstrates an approach for micro-harvesting thermoelectric device applications without the difficulties faced for dimensional up-scaling in alternative Si thermoelectric approaches. Challenges surrounding the thermal budget required for post implant dopant activation in p-type Si are also shown.

Keywords: thermoelectric; silicon; thermal conductivity; thin-film; vacancy

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Nomenclature

S	Seebeck coefficient
T	Temperature
k	Thermal Conductivity
ρ	Electrical Resistivity

1. Introduction

Thermoelectric generators using thin film materials with thicknesses in the range of 1-20 μm are expected to find increasing demand in modern applications. Silicon (Si) offers significant potential for such micro-harvesting devices. It is abundant, easily obtainable and non-toxic with established manufacturing knowledge and track record. Such advantages suggest silicon can provide a complimentary addition to existing commercial thermoelectric materials, particularly for volume based products.

For power generation, micro-harvesting devices require thin film materials to possess suitable values for both power factor and thermal conductivity. With power factor equal to S^2/ρ , the relationship to these properties can be given via the dimensionless figure of merit ZT

$$ZT = \frac{S^2 T}{\rho k} \quad (1)$$

Although highly doped Si has a power factor comparable to commonly used bismuth telluride, thermal conductivity for bulk Czochralski grown Si is approximately 100 times greater. As a result, values of ZT achieved by Si are significantly less (~100 fold) [1] than values of ZT attainable using current commercial materials $(ZT \approx 1)$

Significant reductions in values of thermal conductivity in Si have been demonstrated through nano-structuring approaches such as Si nanowires [2,3] and holey silicon [4]. Such techniques utilise reduced material dimension and structural complexity to produce a filtering or scattering of phonon modes associated with thermal transport.

The reduction of associated phonon mean free path achieves effective reductions in values of k however significant challenges exist for material up-scaling.

With lattice vacancy concentrations ~ 1.5% theoretically predicted to reduce thermal conductivity in bulk Si by ~ 95% [5], an approach using defect engineering to achieve vacancy supersaturations was proposed [6]. In our previous work, large concentrations of point and extended defects were successfully introduced into a silicon-on-insulator (SOI) wafer containing a phosphorus dopant species by high energy ion implantation. This self-implantation of Si ions created a net vacancy rich region extending across the SOI wafer top layer and beyond an isolating buried oxide layer. Following rapid thermal treatment at 600 °C, an almost complete restoration of power factor was achieved in this 100 nm top layer. Thermal conductivity remained significantly reduced - by a factor of 20 compared to values for bulk Si - for short duration annealing due to the disruption of phonon mode thermal transport. ZT was shown to be increased 20 fold over bulk materials.

Following successful demonstration of reduced thermal conductivity via vacancy introduction, it was proposed that this defect engineering technique could be up-scaled to thin film materials [7]. The penetration depth of any extended region containing net vacancy type defects introduced via a high energy ion implantation process was shown via TCAD simulation to be a function of implant energy. Simulation results suggested that such an approach would be scalable to thin film dimensions allowing production of materials suitable for micro-harvesting devices without the up-scaling challenges of current nano-structuring alternatives.

Here we demonstrate experimental up-scaling by applying our defect engineering technique to a SOI wafer with a Si device layer in the thin film thickness range. By increasing implant energy over previous experiments, defect supersaturations are created for an extended range in the SOI wafer.

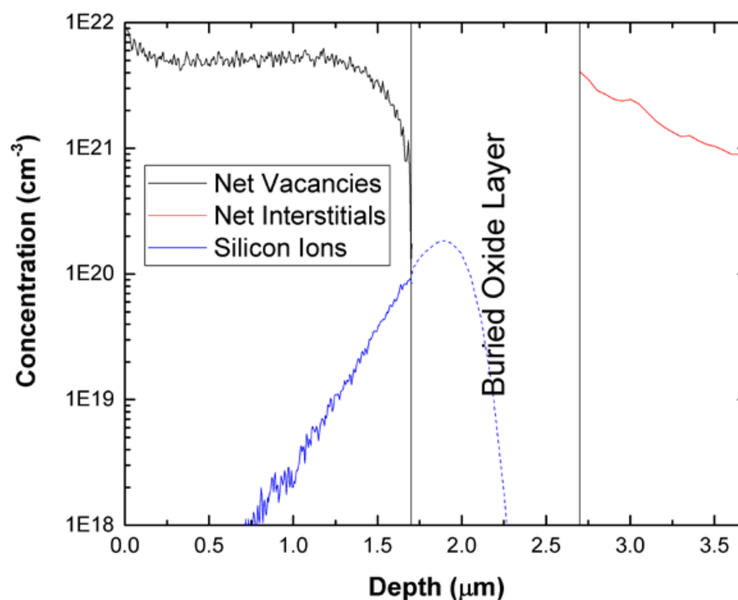

Fig. 1. Silvaco TCAD simulation results showing concentrations of net vacancies, net interstitials and implanted Si ions as a function of depth in an SOI wafer

In line with previous experiments, spatial separation of created vacancy and interstitial pairs due to transference of forward momentum remains. Local recombination of vacancies and interstitials post implant creates a wafer top layer featuring a net vacancy concentration. This net vacancy region extends into a layer of buried oxide within the SOI wafer while a region featuring a corresponding net concentration of interstitials is created behind this isolating barrier.

2. Experimental Design

Silvaco Athena TCAD software [8] was employed to define experimental conditions suitable for ion beam implantation at University of Surrey's Ion Beam Centre. Such software enables an investigation of point defect concentration levels and spatial displacement created by a self-implantation of Si on SOI wafer.

Net defect distribution $\left(C(x)\right)$ is calculated via $C(x) = Si(x) + I(x) - V(x)$, a modified version of the Net Recoil Density algorithm [9]. These TCAD simulations predict that net vacancy region depth penetration of 1.8 μm is possible for the 2 MeV implant energy available. Fig. 1 shows simulated defect distribution as a function of depth for an SOI substrate (1.7 μm Si / 1 μm SiO_2 / 500 μm Si) after an implant of 100,000 ions at 300 K. Implant fluence of 8 x 10^{15} cm^{-2} was selected to introduce high post implant defect concentration levels without introducing amorphisation.

A large net vacancy concentration can be seen extending from the surface of the SOI wafer (0 μm) to the buried oxide layer (1.7 μm) following local recombination. Integrating under the curve for this 1.7 μm thick Si device layer yields a net vacancy density of 8.12 x 10^{17} cm^{-2} and an average net vacancy concentration of 4.78 x 10^{21} cm^{-3}. This can be equated as a 9.6% vacancy concentration, significantly in excess of naturally occurring levels. It should be noted that the TCAD simulation considers mono-vacancies. These are known to be mobile at room temperature and it can be expected that di-vacancy clusters – known to be stable at room temperature – are instead likely to be dominant within the region identified by simulation [10].

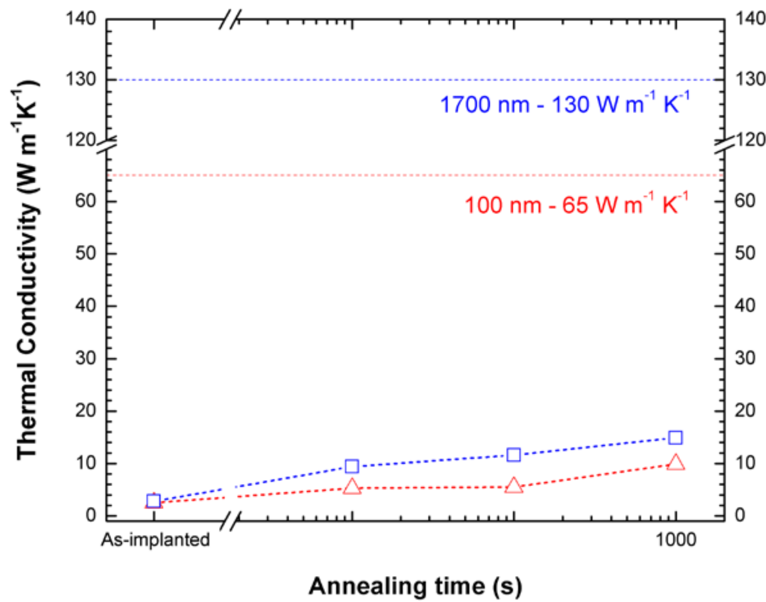

Fig. 2. Cross plane thermal conductivity at room temperature as a function of annealing time at 600 ºC for i) silicon-on-insulator samples (1.7 µm Si / 1 µm SiO_2 / 500 µm Si) subjected to high energy Si ion implantation (2 MeV, 8 x 10^{15} cm^{-2}) shown as blue squares and for ii) silicon-on-insulator samples (100 nm Si / 200 nm SiO_2 / 300 µm Si) subjected to Si ion-implantation (1 MeV, 5 x 10^{15} cm^{-2}) shown as red triangles. Written values represent thermal conductivity for samples not exposed to vacancy engineering.

3. Experimental Methods

As with previous work, the use of an SOI wafer enables separation of post implant vacancy and interstitial concentrations. The layer of buried oxide acts as a physical barrier preventing cross boundary migration and therefore recombination during post implant thermal treatment. Straightforward characterisation of the isolated top layer of Si is also facilitated. Samples were manufactured using a <100> SOI wafer containing a boron dopant species. This 100 mm diameter SOI wafer consisted of an Si device layer ~1.7 μm thick (p-type, ≤ 5 mΩ-cm) above a layer of buried oxide with thickness 1 μm and a Si handling substrate ~ 500 μm thick. Characterisation of resistivity, carrier concentration and doping type were undertaken at room temperature using a Bio-Rad HL5900+ Hall profiler using Hall-effect and Van der Pauw resistance measurements. Ion implantation was carried out at University of Surrey's Ion Beam Centre using a Varian VIISta ion implanter at a beam energy of 2 MeV with a fluence of 8 x 10^{15} cm^{-2}. Post-implant, the SOI wafer was diced into pieces approximately 10 mm x 10 mm before undergoing rapid thermal annealing (RTA) in a nitrogen environment using a Jordan Valley Bede D1 in conjunction with an Anton Paar TCU 200 temperature controller. Samples were annealed using a combination of isochronal and isothermal conditions – 10,100 and 1000 seconds, 600 - 1000 ºC – before undergoing further characterisation. Cross plane thermal conductivity for the Si device layer was obtained using a 2-omega system via a commercial vendor.

4. Results and Discussion

4.1 Thermal Conductivity

Fig. 2 shows corresponding values of cross plane thermal conductivity at room temperature as a function of RTA duration at 600 ^oC. Significant reductions in k are shown as a result of high energy ion implantation.

Thermal conductivity in the as-implanted sample is found to be 2.8 W m^{-1} K^{-1} as a result of damage introduced during the 2 MeV implant. With implant fluence of 8 x 10^{15} cm^{-2} selected to maximise damage without achieving sample amorphisation such a value for thermal conductivity - being slightly greater than the amorphous limit - is in line with expectations [11].

The application of isothermal annealing is shown to increase thermal conductivity over this as-implanted value. An RTA of 10 seconds is found to correspond to a sample thermal conductivity of 9.4 W m^{-1} K^{-1} while an RTA duration of 100 seconds produces a value for thermal conductivity of 11.6 W m^{-1} K^{-1}.

After undertaking a longer RTA of 1000 seconds duration, sample thermal conductivity was found to have increased to 14.9 W m^{-1} K^{-1}. This remains almost an order of magnitude lower than for values expected for silicon of comparable thickness (1700 nm) demonstrating significant reductions in k remain even after this extended RTA duration.

These trends are in line with previous experiments undertaken using a SOI wafer featuring a 100 nm device layer and subjected to a similar high energy self implantation process. In the case where the Si layer is upscaled from 100 nm to 1700 nm, a small increase in thermal conductivity can be seen for each annealing condition. This could result from one of two factors. Firstly, the implant conditions used in each case are different. If the 100 nm wafer contained a greater density of defects post implant it is likely that recovery of thermal conductivity during annealing will be slower. Secondly, that layers are simply of considerably different thicknesses. Since thermal conductivity is similar for both sample thicknesses in the as-implanted condition, it is likely that differences result directly from the reduced thickness of the 100 nm layer.

4.2 Resistivity

Fig. 3(a) shows sample resistivity in response to a series of isochronal and isothermal RTA's. Sample values following an isochronal RTA process with a 10 second duration can be seen via blue squares, while those produced via an isothermal RTA at 600 ^oC for durations of 100 and 1000 seconds corresponding to conditions shown in Fig. 2 for thermal conductivity are also shown.

It can be seen that isothermal anneal conditions of 10, 100 and 1000 seconds are insufficient to restore resistivity values to those of control sample at 5 mΩ cm. Indeed the value of resistivity after exposure to 600 ^oC at 1000 seconds – 48.5 mΩ cm – remains almost a magnitude greater than for pre-implant samples.

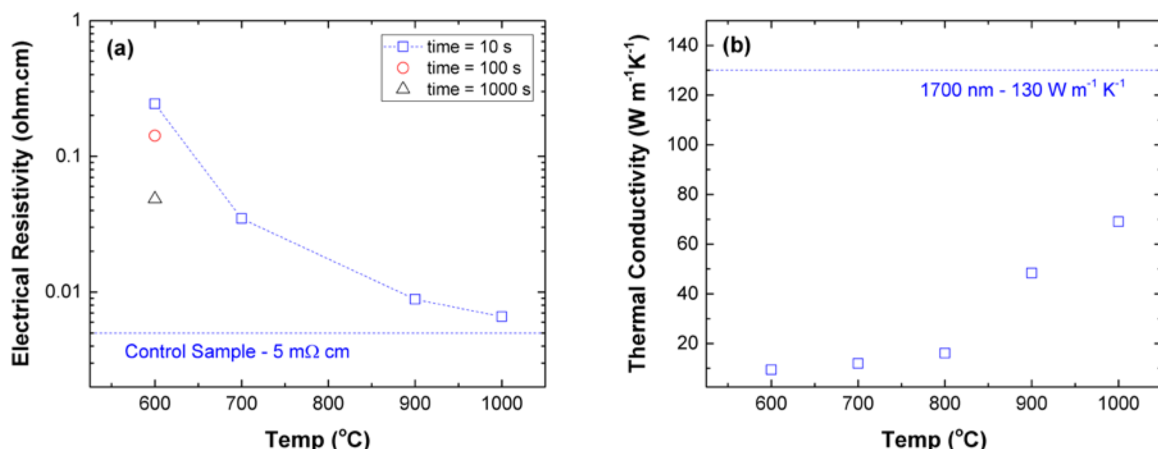

Fig. 3. (a) Electrical resistivity as a function of both annealing temperature and duration for silicon-on-insulator samples (1.7 μm Si / 1 μm SiO_2 / 500 μm Si) subjected to high energy Si ion implantation (2 MeV, 8 x 10^{15} cm^{-2}), and (b) Cross plane thermal conductivity in the Si layer as a function of annealing temperature for an RTA duration of 10 second. Measurements were made at room temperature.

A series of isochronal RTA's featuring a duration of 10 seconds and increasing thermal budget were undertaken to establish conditions for complete restoration of sample resistivity. Increasing RTA temperature can be seen to result in a decrease in sample resistivity with an RTA temperature of 1000 ^oC and 10 second duration was found to restore values of resistivity almost to that of control.

Fig. 3(b) shows the effect of these isochronal RTA conditions on sample thermal conductivity. The increasing RTA temperature can be seen to produce a corresponding rise in thermal conductivity relative to samples exposed to lower RTA temperatures. Thermal conductivity following a 1000 ^oC 10 second RTA was found to be 69 W m^{-1} K^{-1}. While this remains almost half that of values typical for silicon of comparable thickness, it can be seen to be significantly increased over values achieved for RTA temperatures up to 800 ^oC at 10 seconds – 16.1 W m^{-1} K^{-1} - and those achieved following a 600 ^oC RTA for 1000 seconds - 14.9 W m^{-1} K^{-1}.

In line with previous results, increased thermal budget can be expected to lead to i) defect evolution including an increased vacancy cluster size and ii) defect reduction as vacancies are lost at sinks such as the buried-oxide and surface interfaces [10,12]. Both of these events are predicted via non equilibrium molecular dynamics studies to lead to increased thermal conductivity as phonon mean free path is increased [5]. Sufficient thermal budget can be expected to restore phonon mean free path and thus thermal conductivity to in line with pre-implanted samples.

While previous experiments using an SOI wafer doped with phosphorus were found to experience i) almost complete restoration of electrical properties following an RTA of 600 ^oC for 10 seconds and ii) significant reduction in thermal conductivity for RTA durations up to 1000 seconds for the same 600 ^oC temperature, this was not found to be the case using a boron doped SOI wafer. Reductions in thermal conductivity were found to remain significantly reduced in response to 600 ^oC RTA durations of 10 – 1000 seconds, however such RTA conditions were insufficient to achieve restoration of electrical properties in line with those of the pre-implanted control sample. Boron is known to preferentially form stable defect clusters with silicon self-interstitials requiring an increased thermal budget to free the dopant atom and allow activation. In comparison to phosphorus, boron requires increased RTA temperatures to achieve similar levels of reactivation [13, 14]. At high dopant levels phosphorus is shown to achieve maximum activation for RTA temperatures of 600 ^oC. Maximum activation for boron was only achieved for RTA temperatures in excess of 900 ^oC. That an increased thermal budget – 1000 ^oC, 10 seconds - was found to restore sample resistivity to almost in line with control samples supports this explanation. Work is now on-going to experimentally confirm this hypothesis and investigate solutions to achieve a sufficiently low electrical resistivity alongside low thermal conductivity in p-type silicon.

5. Conclusion

The up-scaling of an approach to reduce thermal conductivity in silicon micro-films via the introduction of lattice vacancy supersaturations was successfully demonstrated. As implanted samples were shown to have values of thermal conductivity approaching the amorphous limit while samples subjected to an RTA of 600 ^oC for 10 and 1000 seconds were shown to have thermal conductivity values approximately 14 and 10 times lower than would be expected for pristine silicon of similar thickness. For any given RTA condition, thermal conductivity values were found to be slightly higher for micro-films than for corresponding nano-films. Such an approach suggests that reductions in thermal conductivity for silicon for use in thermoelectric applications can be achieved without the dimensional up-scaling difficulties encountered for alternative silicon thermoelectric approaches. While we have previously demonstrated this approach successfully in n-type silicon, challenges remain surrounding the thermal budget required for boron dopant activation in p-type silicon.

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